

Makenoise Maths
Manual Patch Ideas illustrated



by Demonam

Voltage Controlled Transient Generator (Attack/ Decay EG)

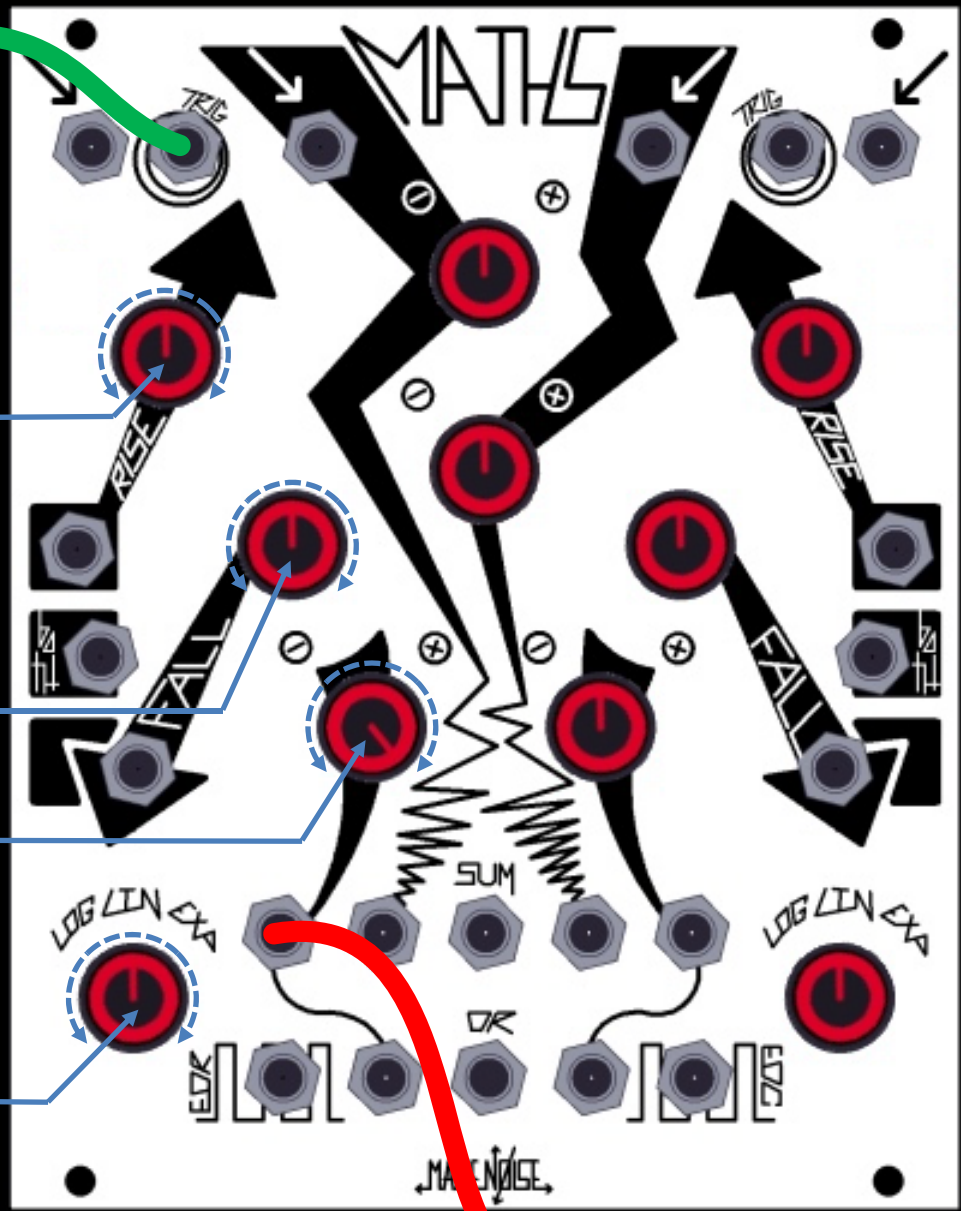
pulse or gate

Attack

Decay

EG scale/inversion

Response



EG Out

Voltage Controlled Sustained Function Generator (A/S/R EG)

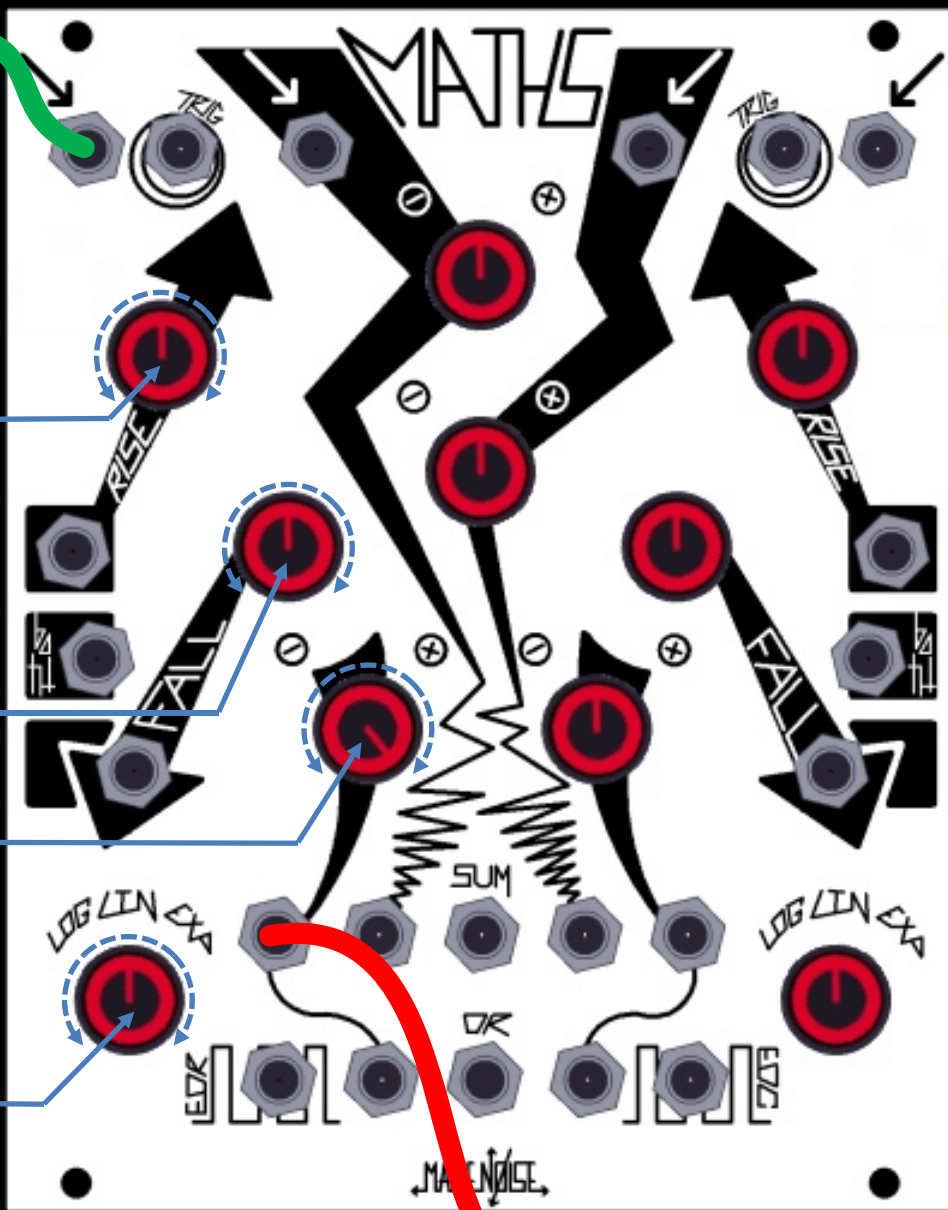
gate

Attack

Release

EG scale/inversion

Response



EG Out

Typical Voltage Controlled Triangle Function

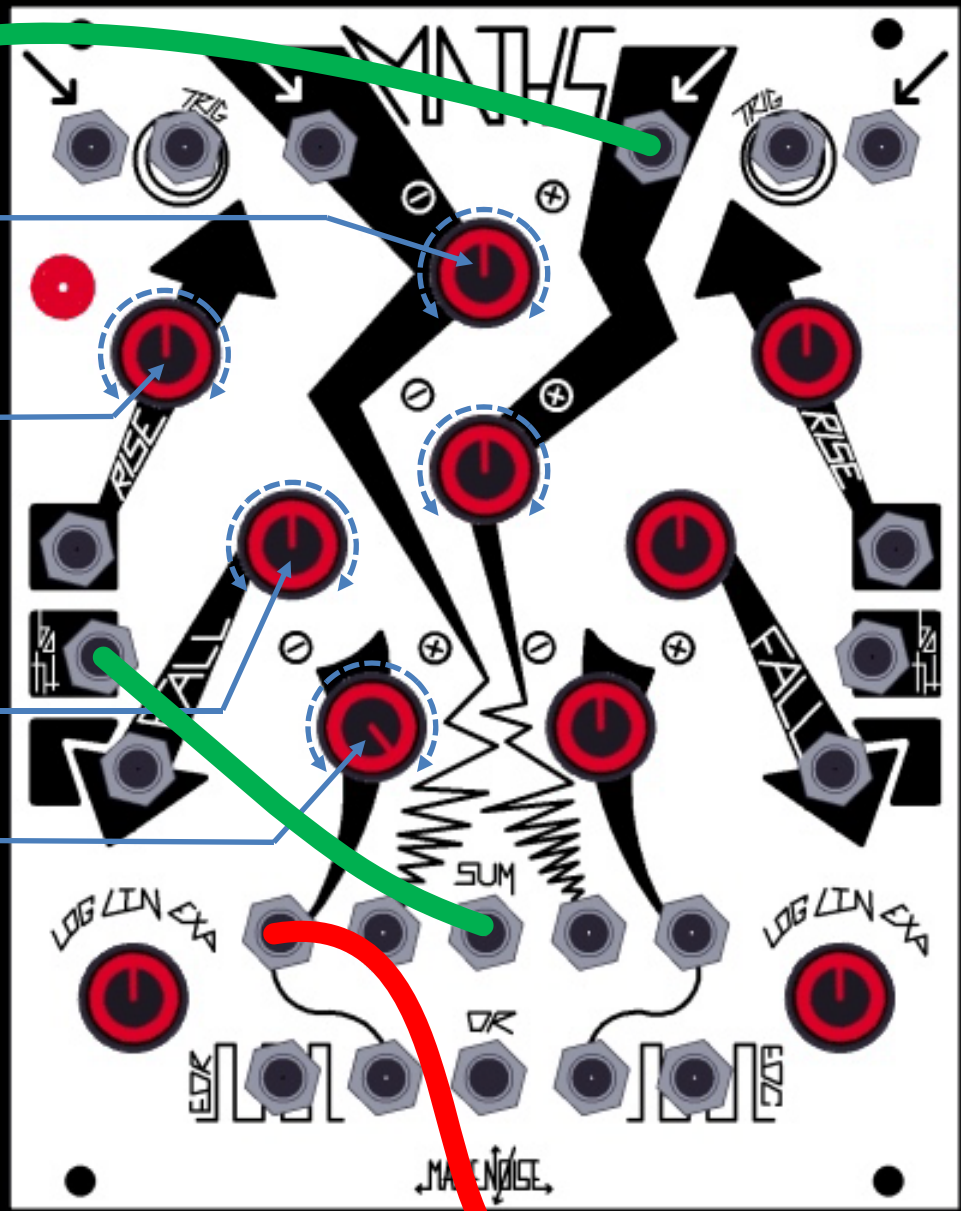
desirated modulation

Frequency

Frequency

Frequency

Out scale/inversion



Out

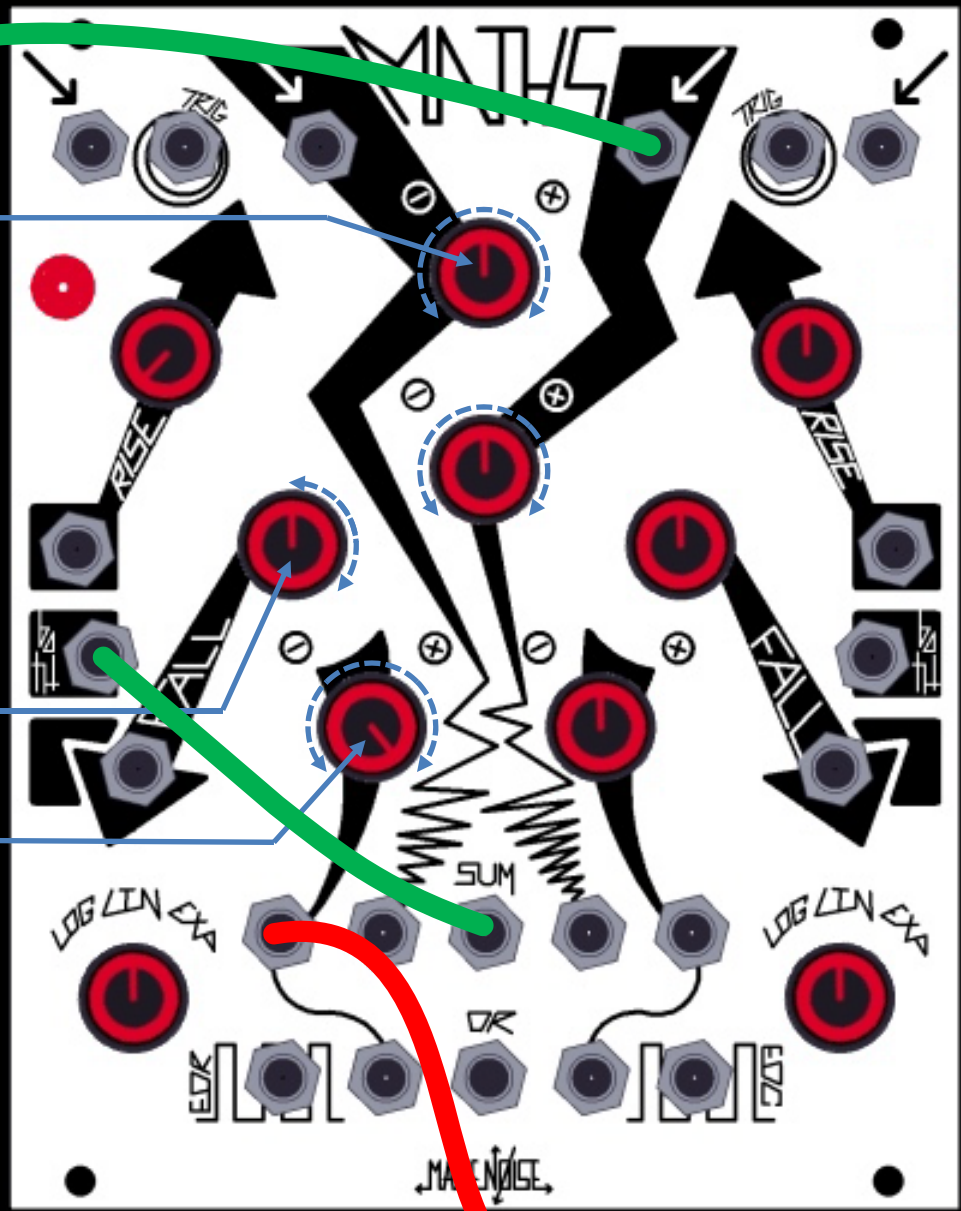
Typical Voltage Controlled Ramp Function

desirated modulation

Frequency

Frequency

Out scale/inversion



Out

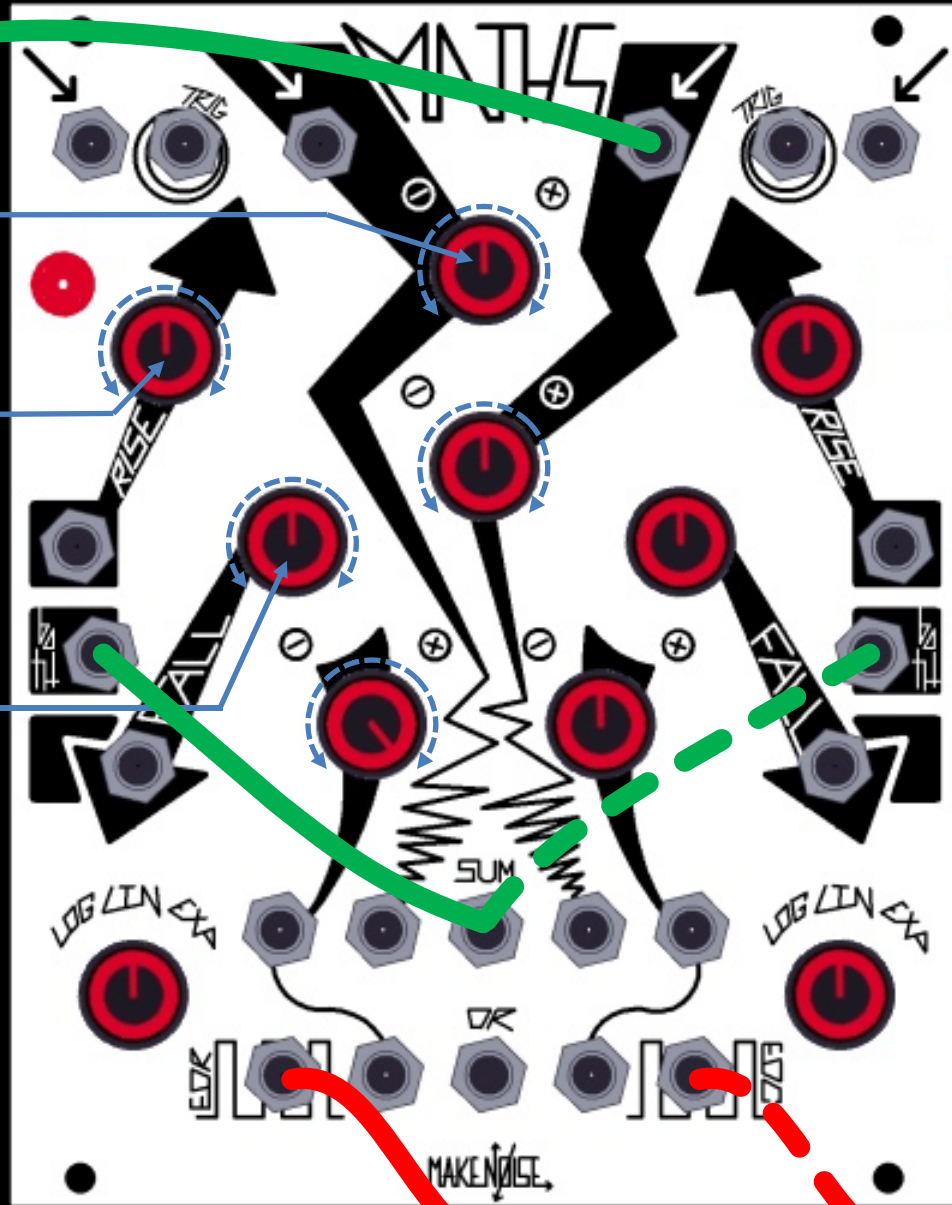
Typical Voltage Controlled Pulse

desirated modulation

Frequency

Frequency

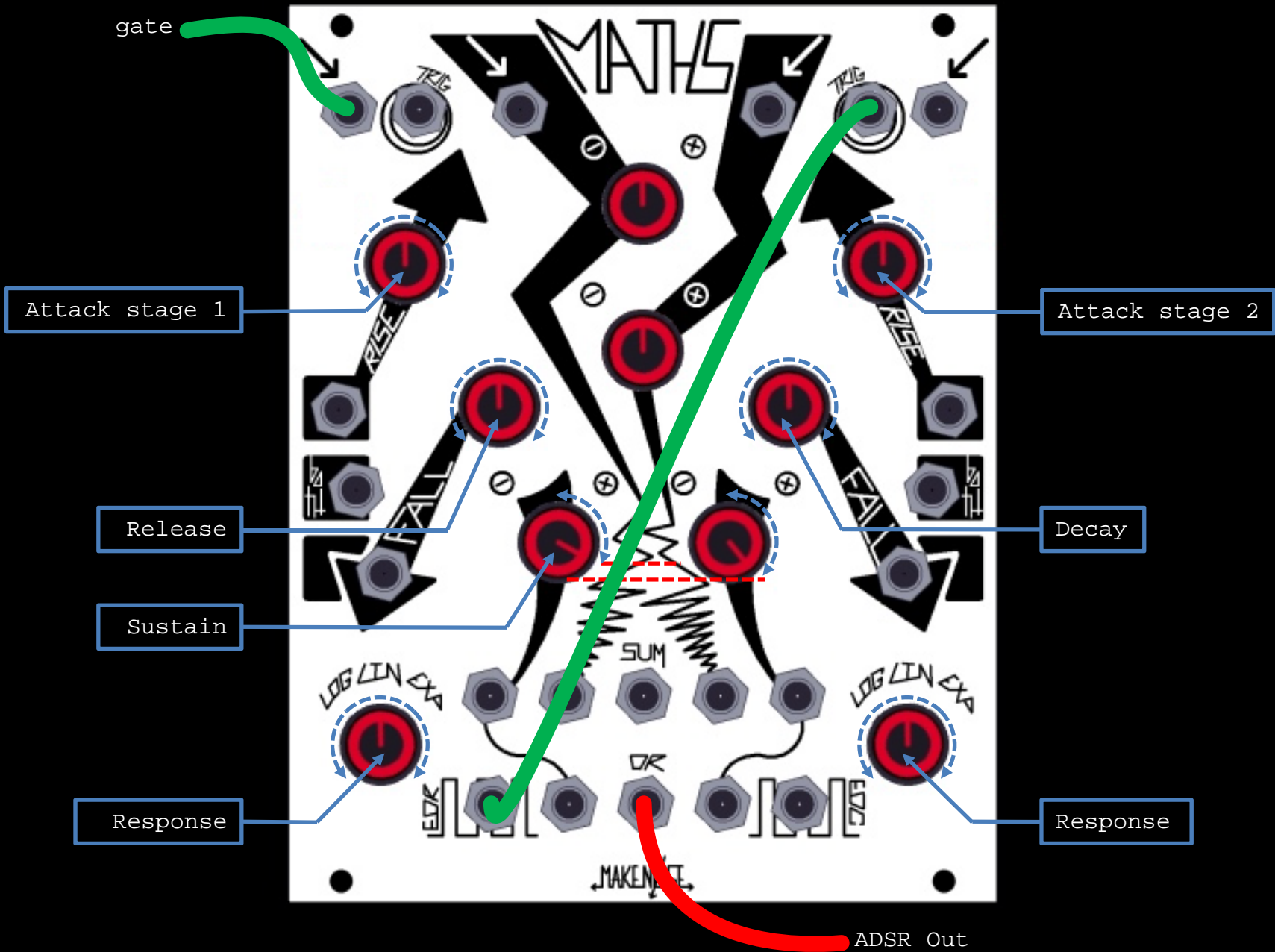
pulse width



Out

Out

Voltage Controlled ADSR (East Coast Envelope done West Coast style)



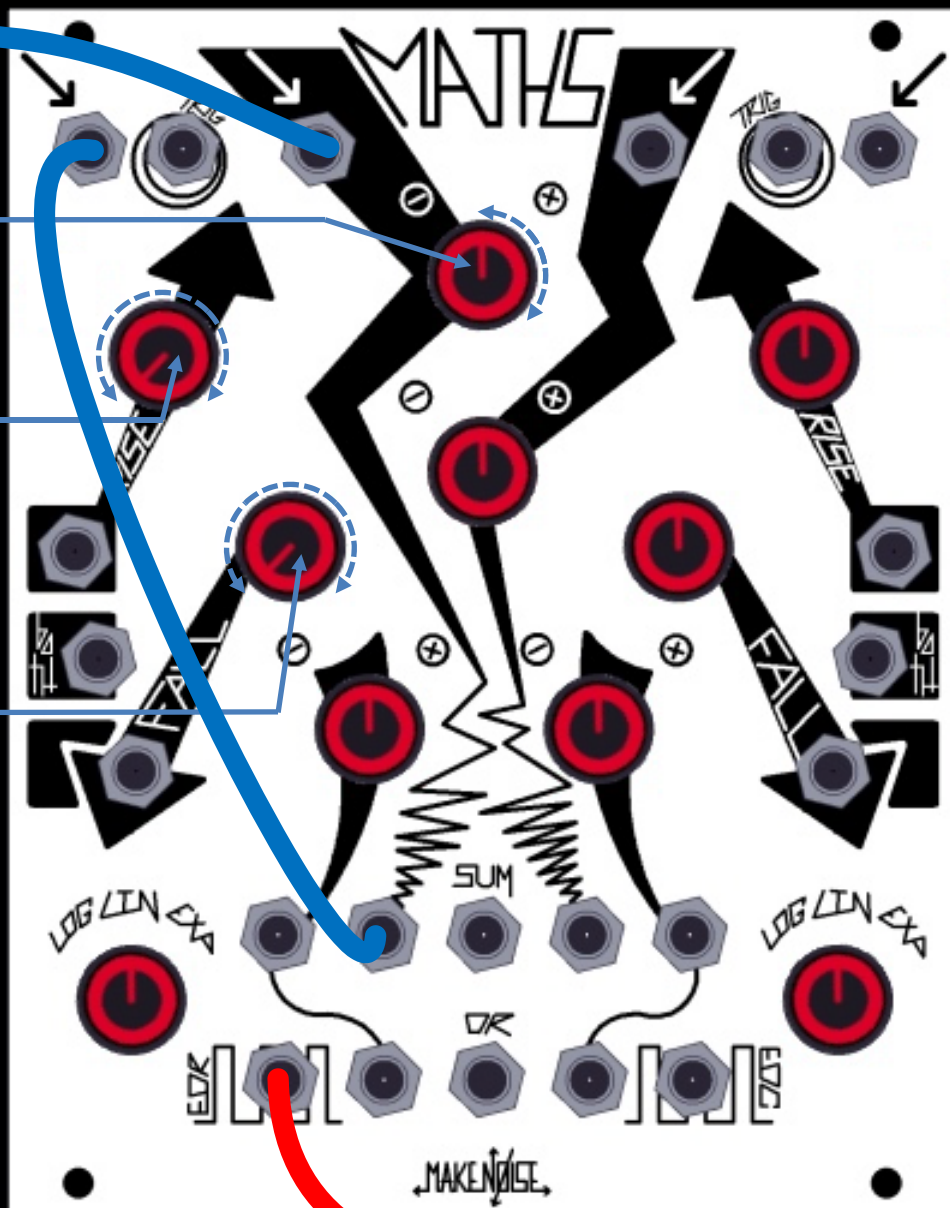
Voltage Comparator/ Gate Extraction w/ variable width

signal to be compared

threshold

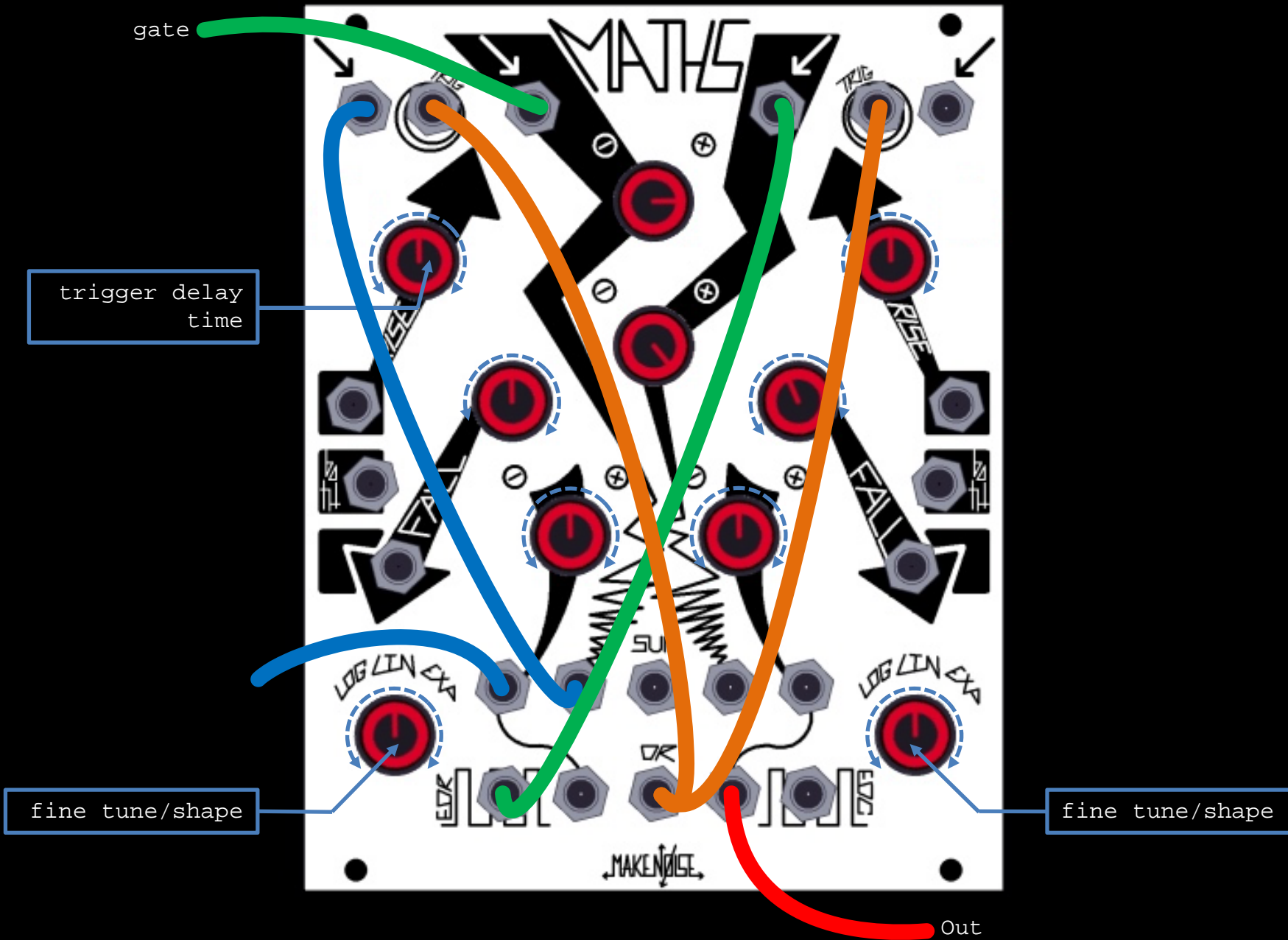
derivate gate Delay

derivate gate Width

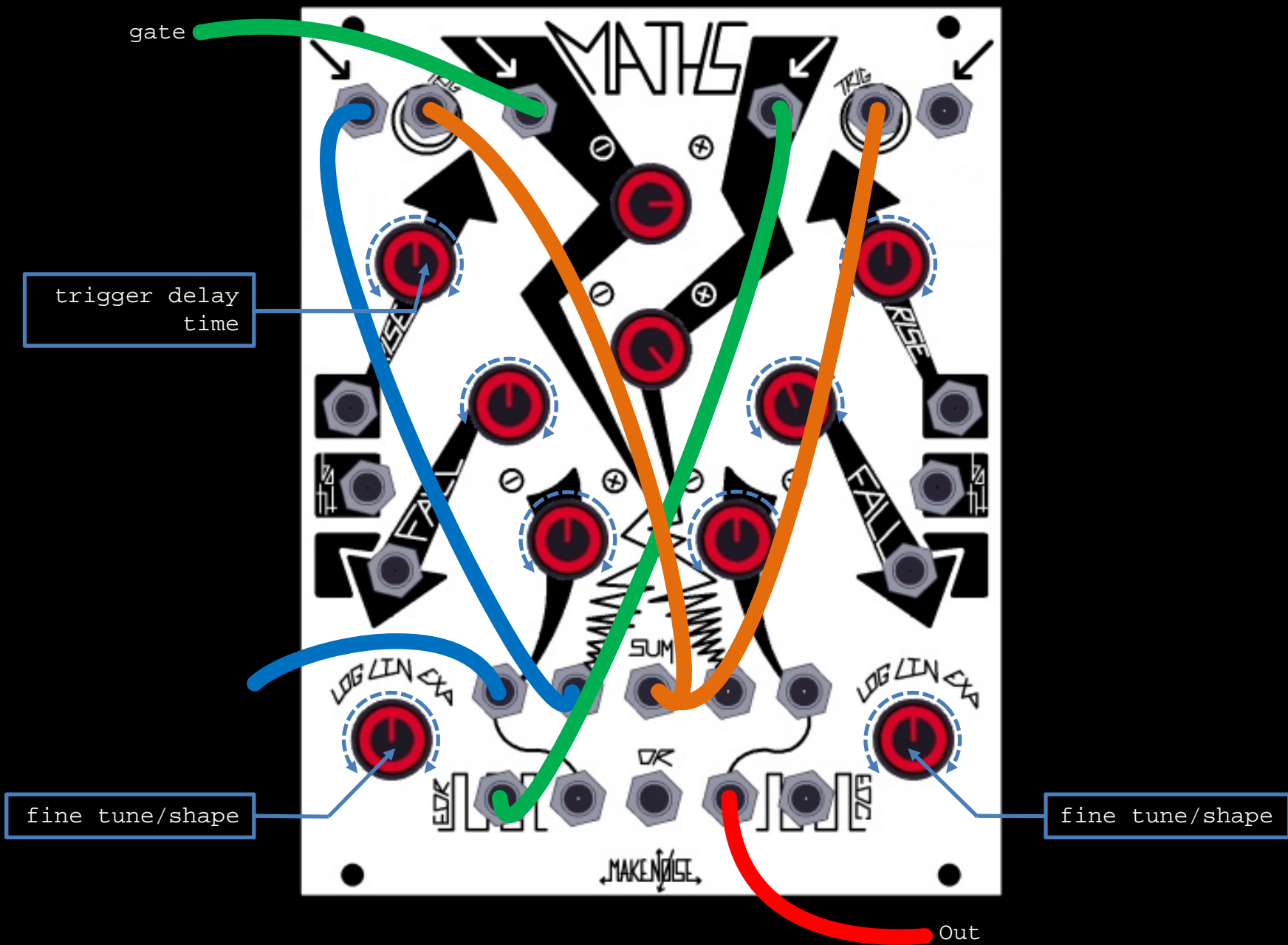


extracted gate

Gate Controlled CYCLE



Toggled Delayed CYCLING



Envelope Follower

signal to be followed



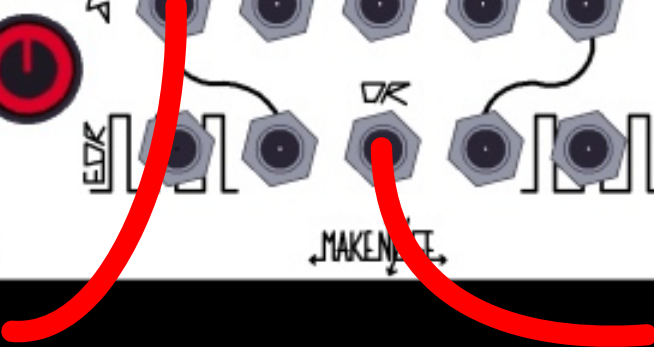
response



scale/inversion

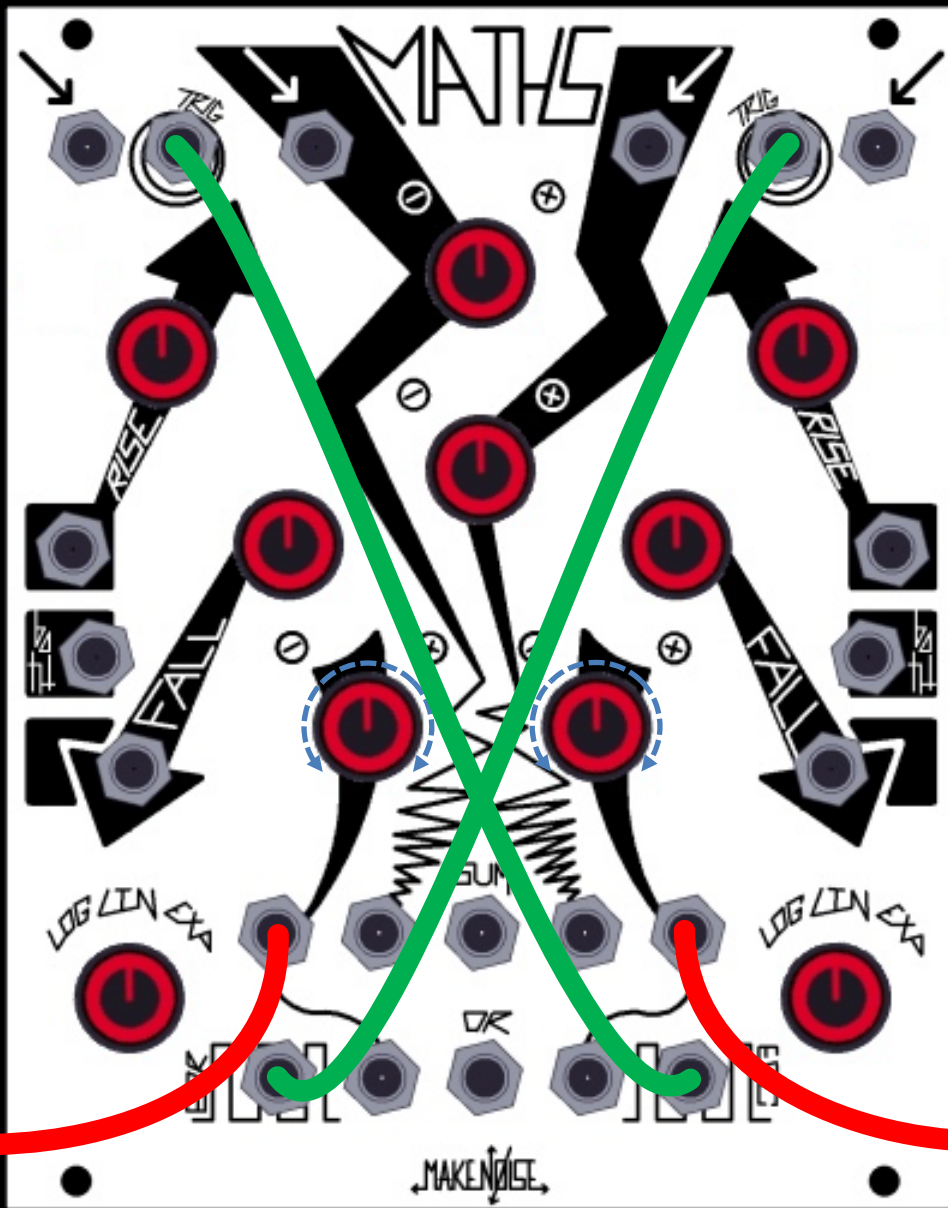


positive/negative Out



positive only Out

281 "Quadrature Mode" (West Coast Swirly Bird)



modulation
destination

modulation
destination

VC LAG/ Slew Processor

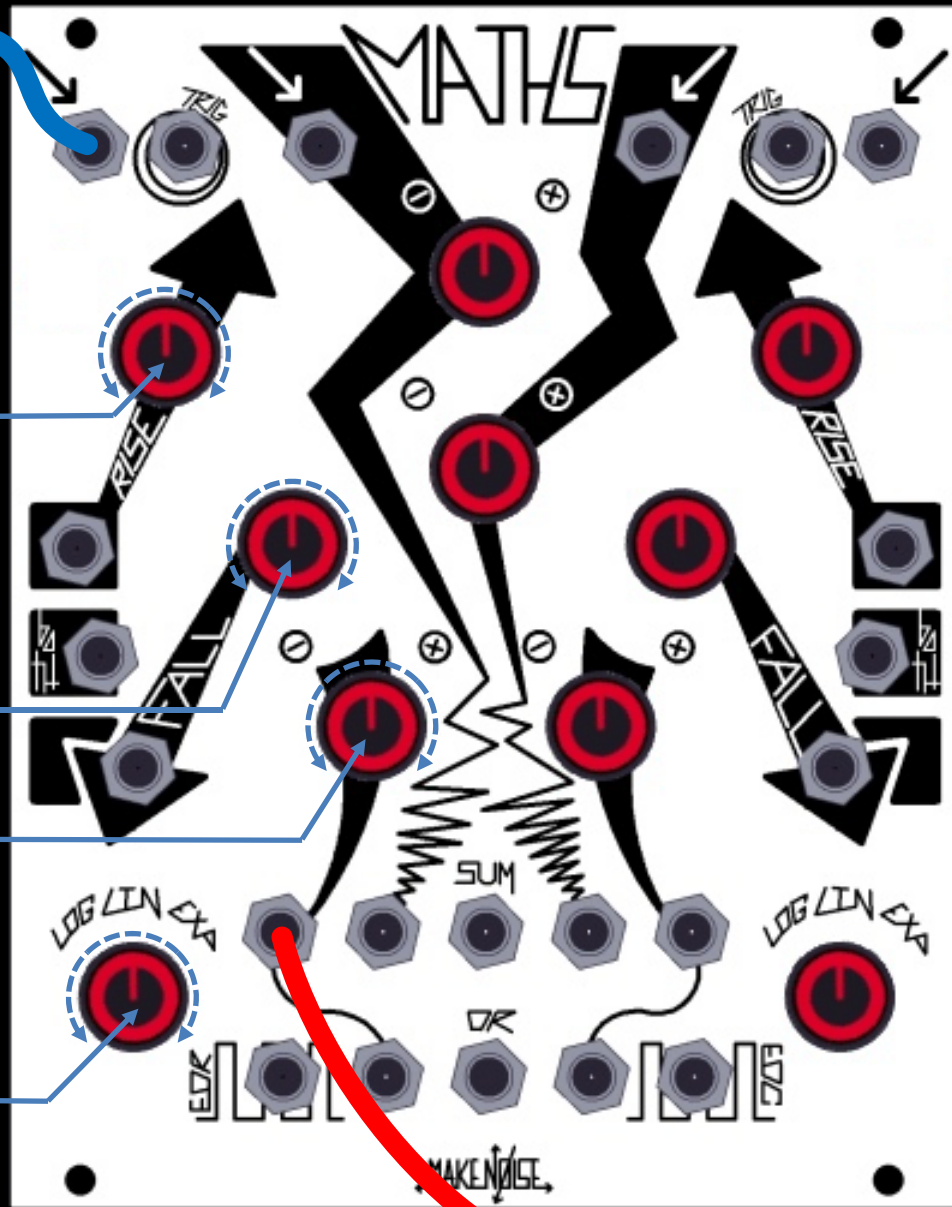
signal to be slewed

slew RISE

slew FALL

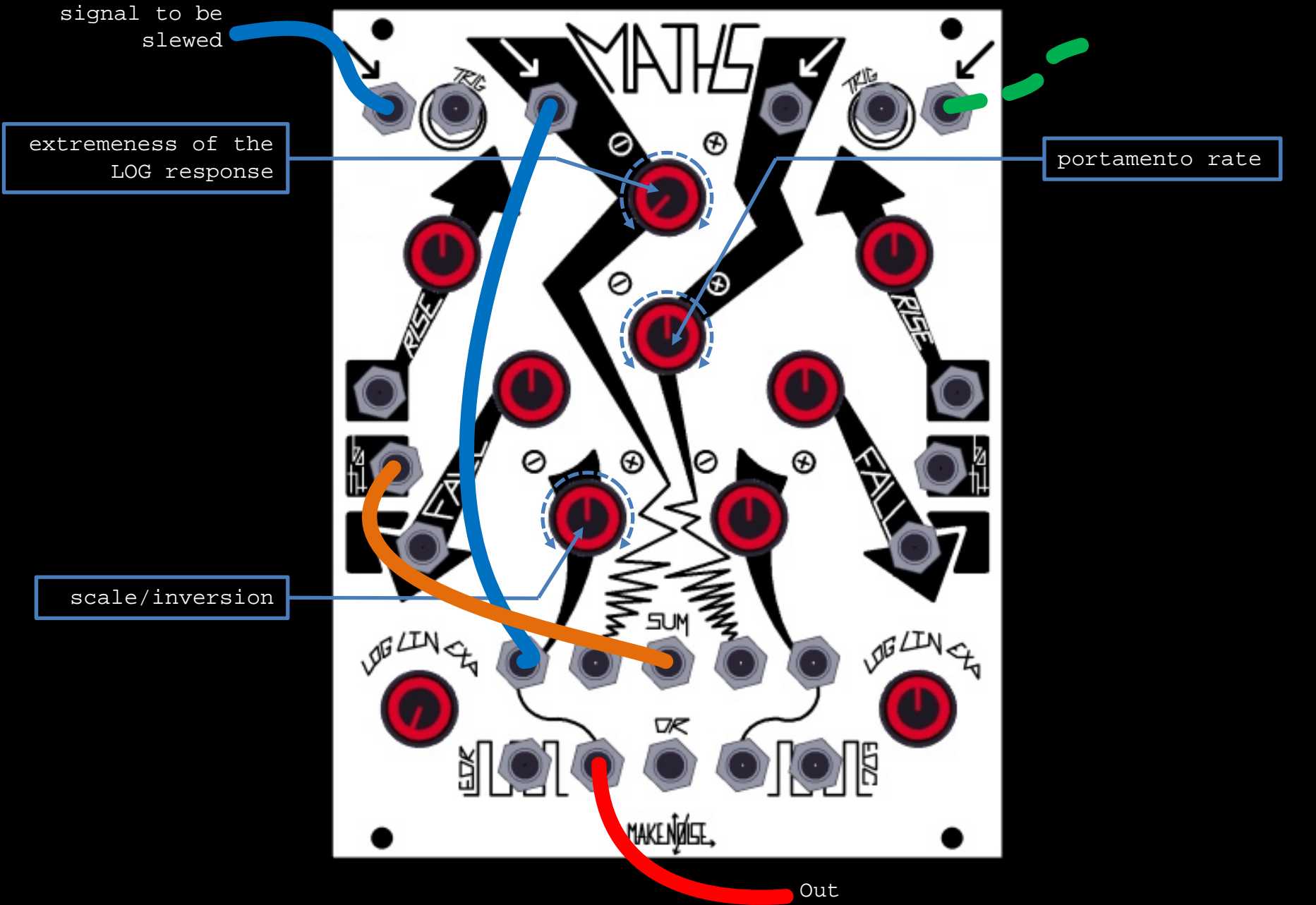
scale/inversion

response

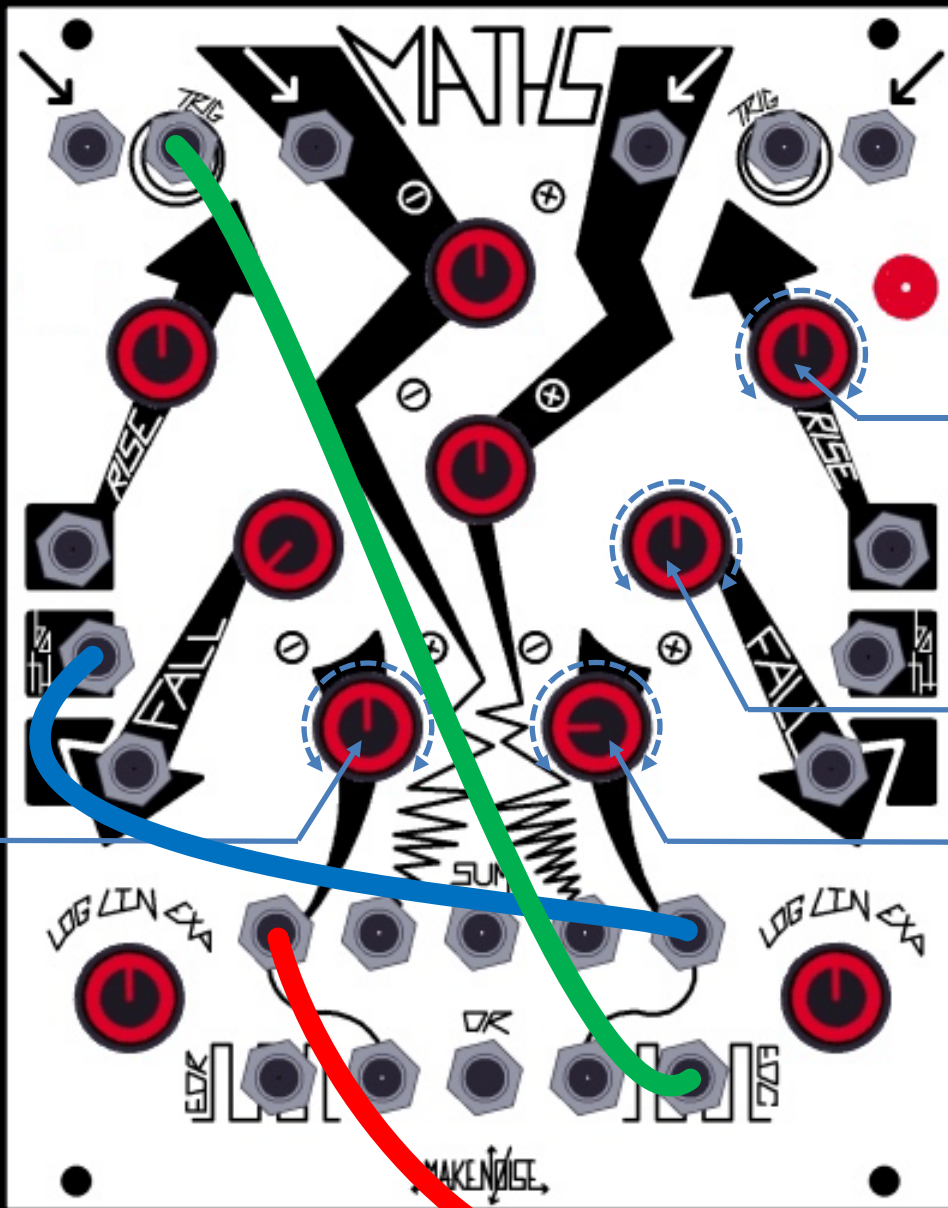


Out

East Coast Portamento



Arcade Trill



trill

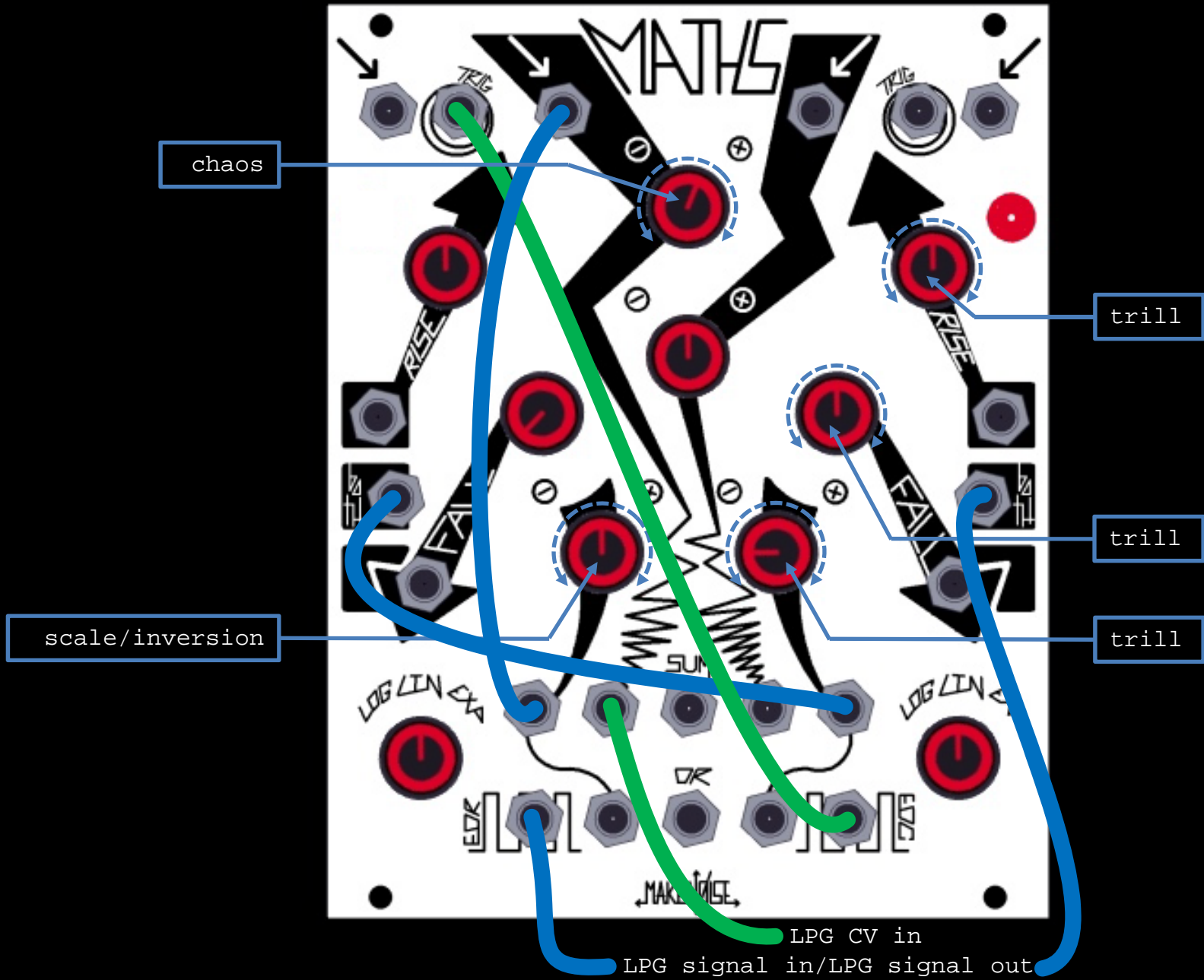
trill

trill

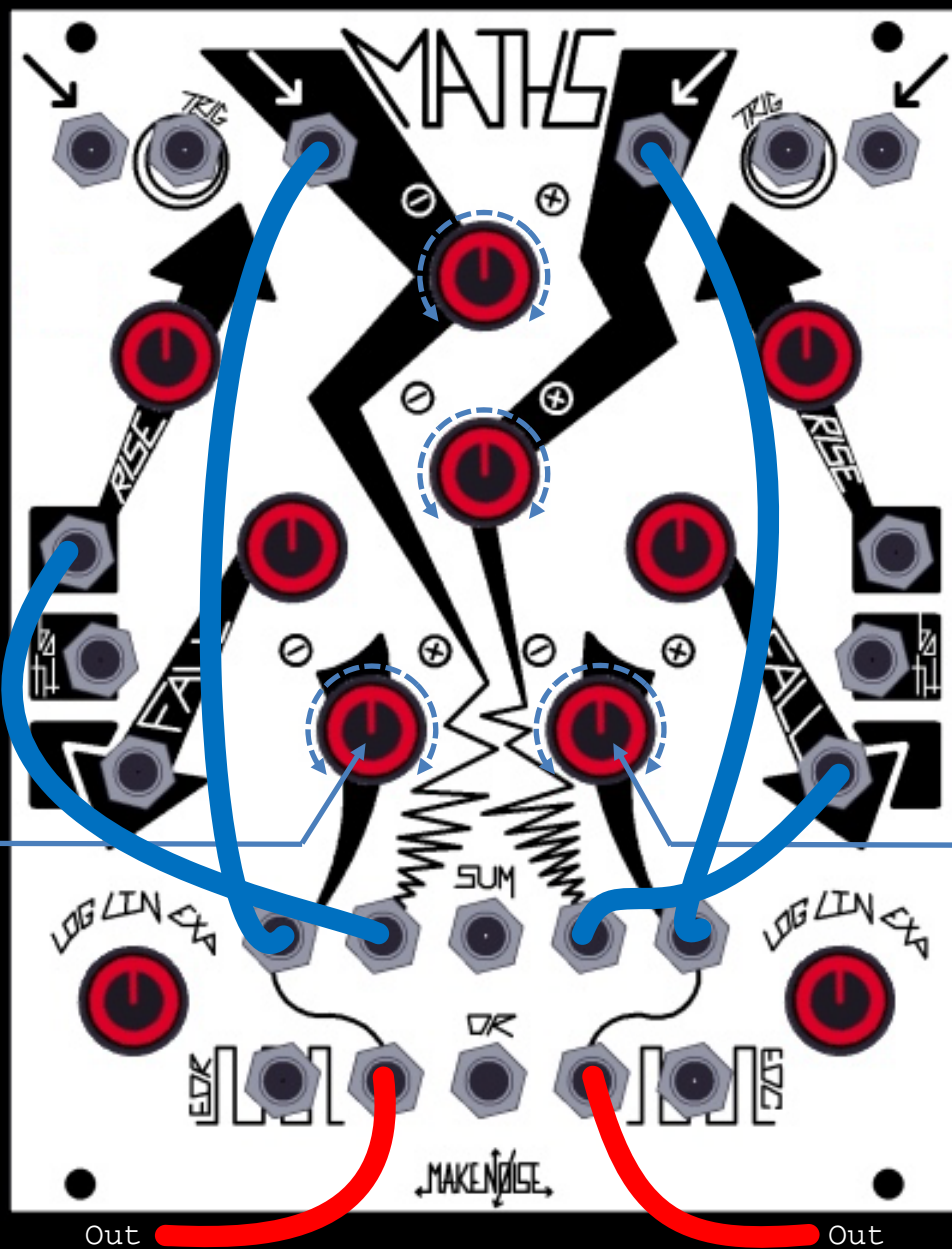
scale/inversion

Out

Chaotic Trill (requires QMMG or other Direct Coupled LP filter)



Independent Contours



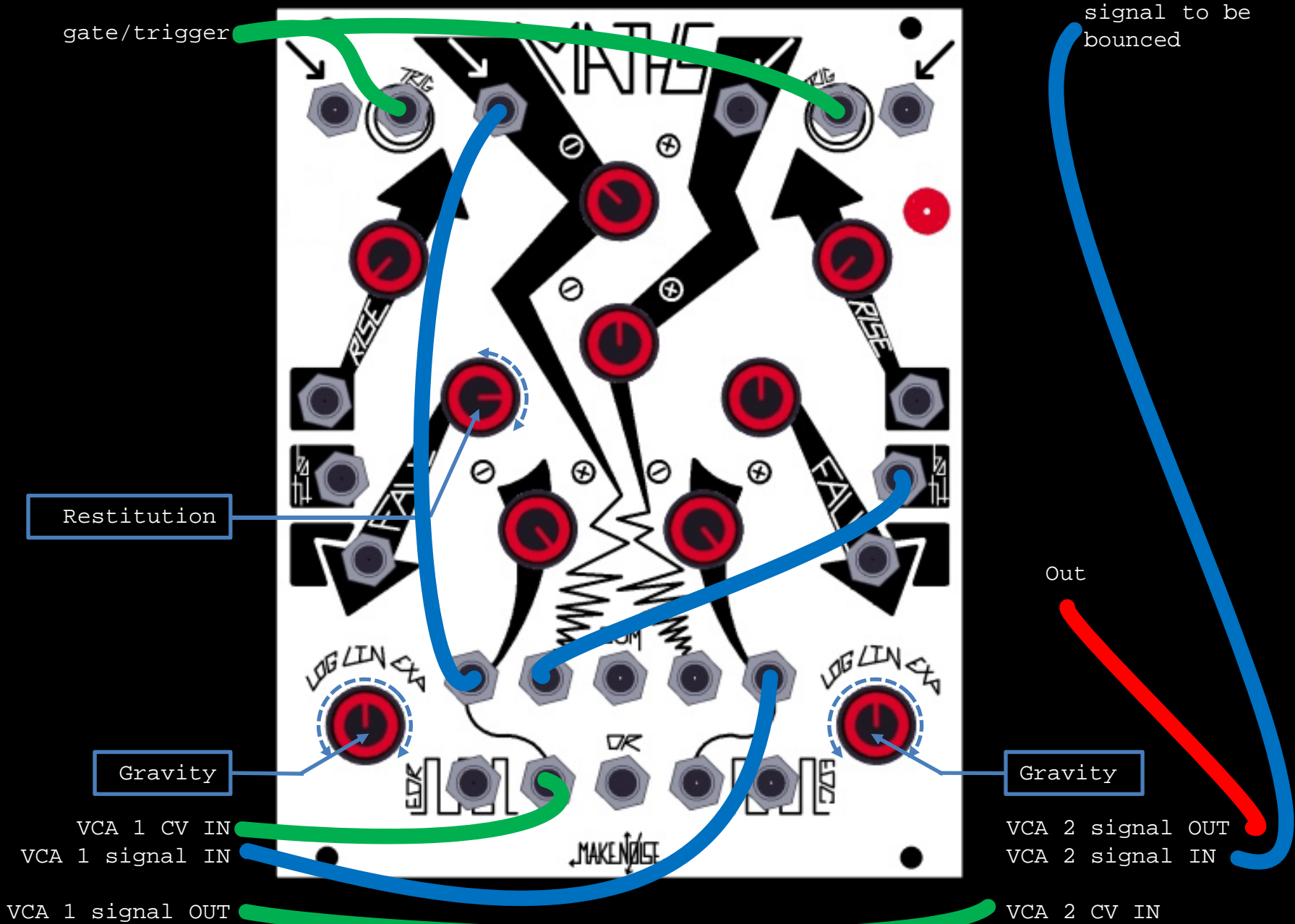
scale/inversion

scale/inversion

Out

Out

Bouncing Ball (requires QMMG or Dual VCA)



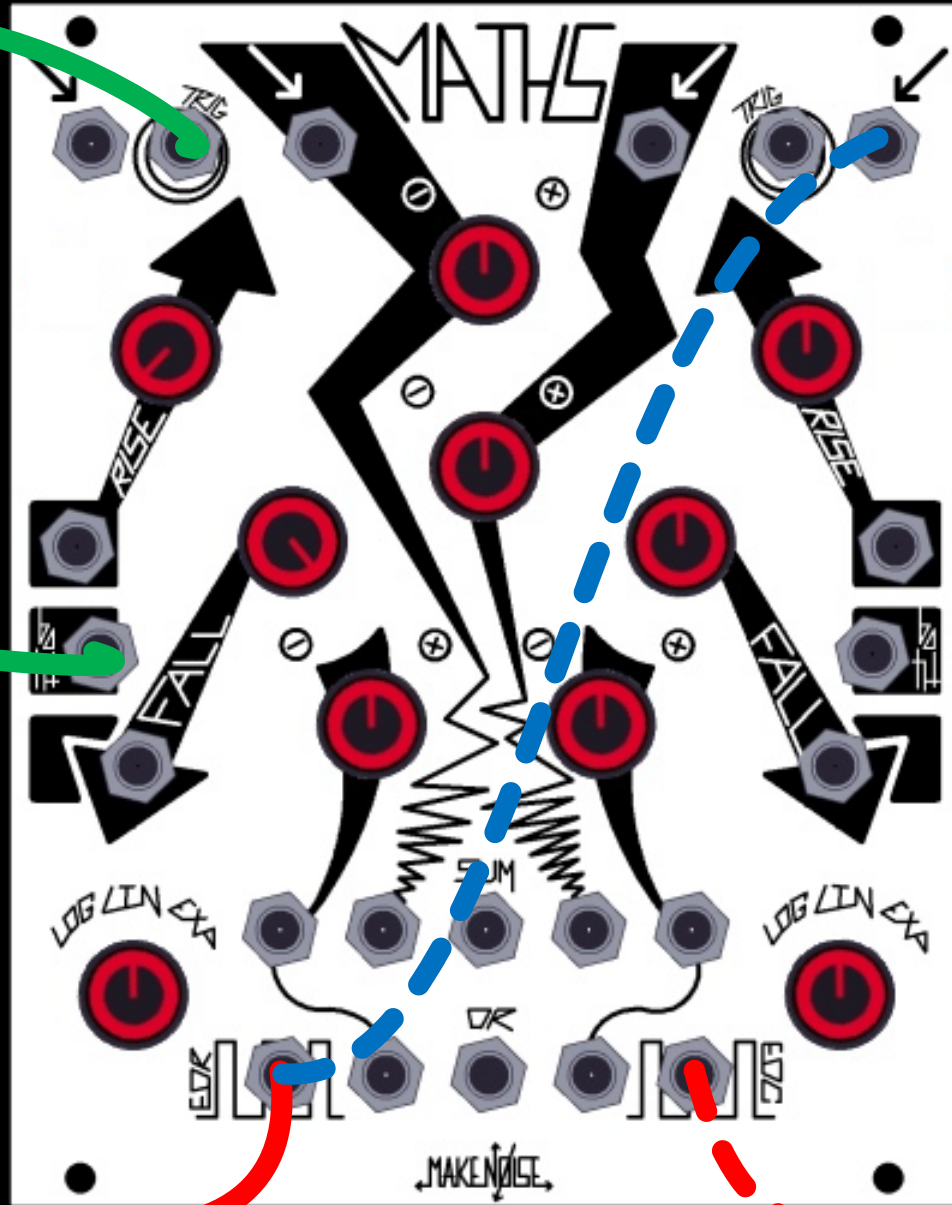
FLIP-FLOP (1-Bit Memory)

Gate/logic

Reset

"Q" Out

"NOT Q" Out



Voltage Controlled Pulse Delay Processor

Trigger or Gate

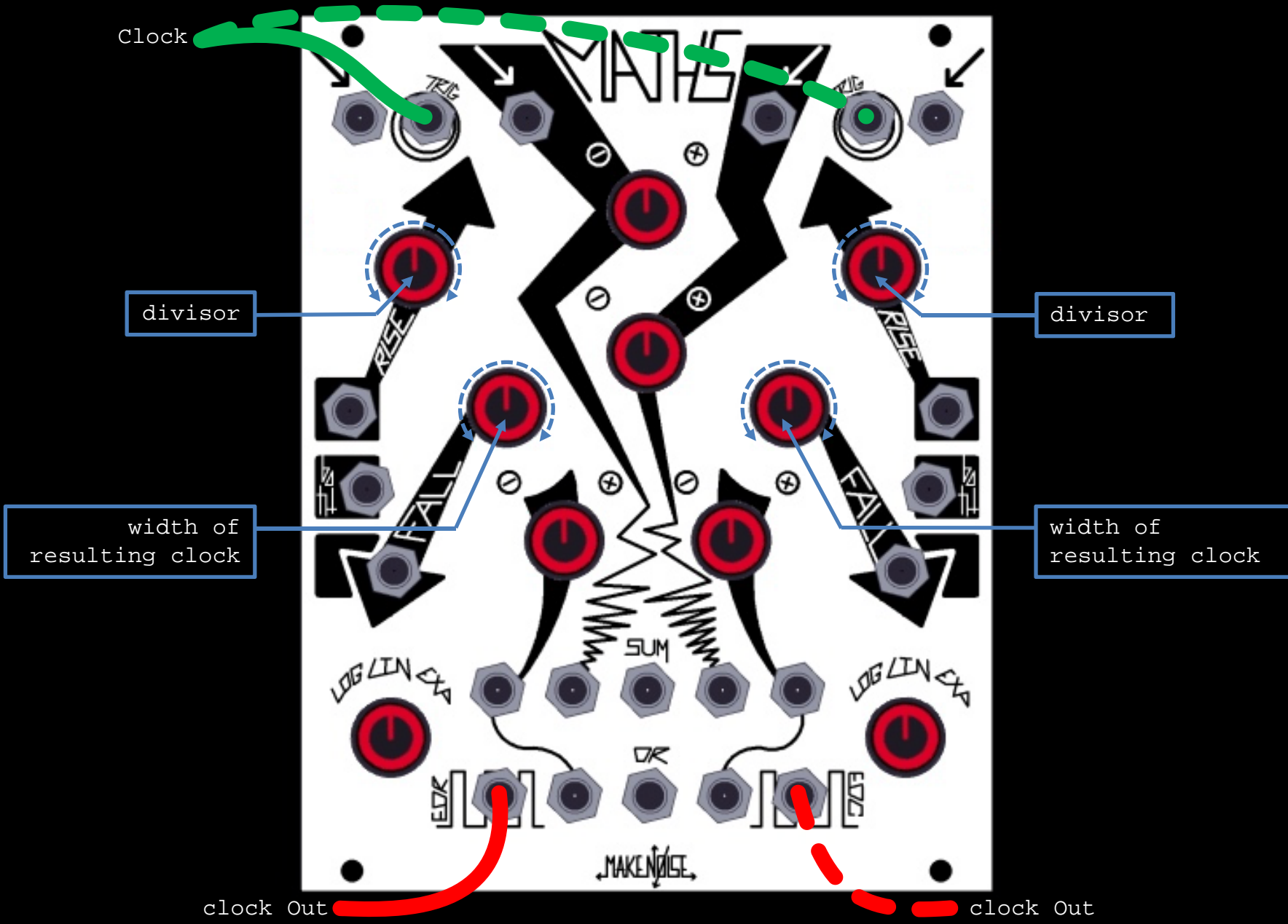
delay

width of
delayed pulse



Out

Voltage Controlled Clock Divider



Logic Invertor



logic gate

Out

Half Wave Rectification

bi-polar signal



Out

Full Wave Rectification

signal to be
rectified

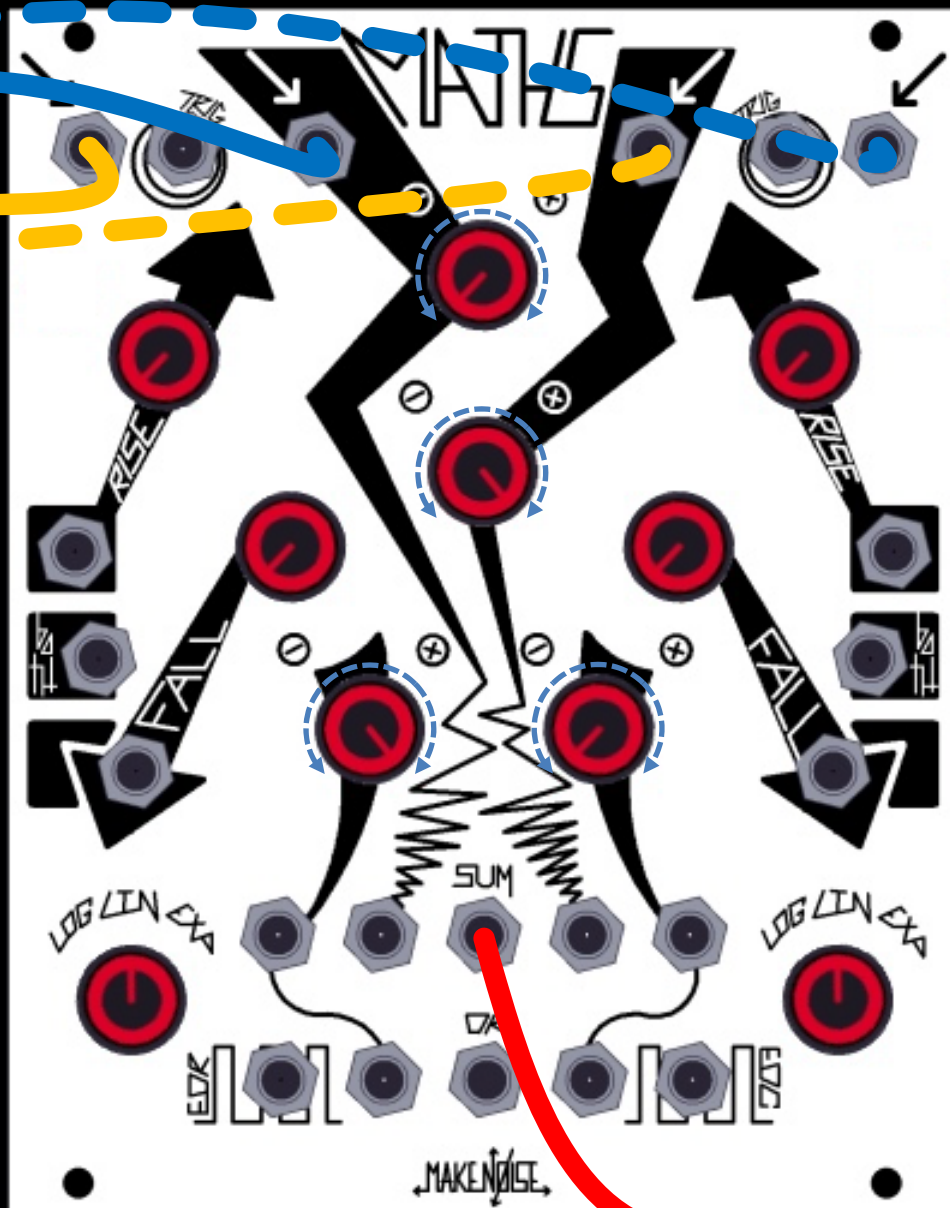


Out

ADD, Subtract Control Signals

signal(s) to be subtracted

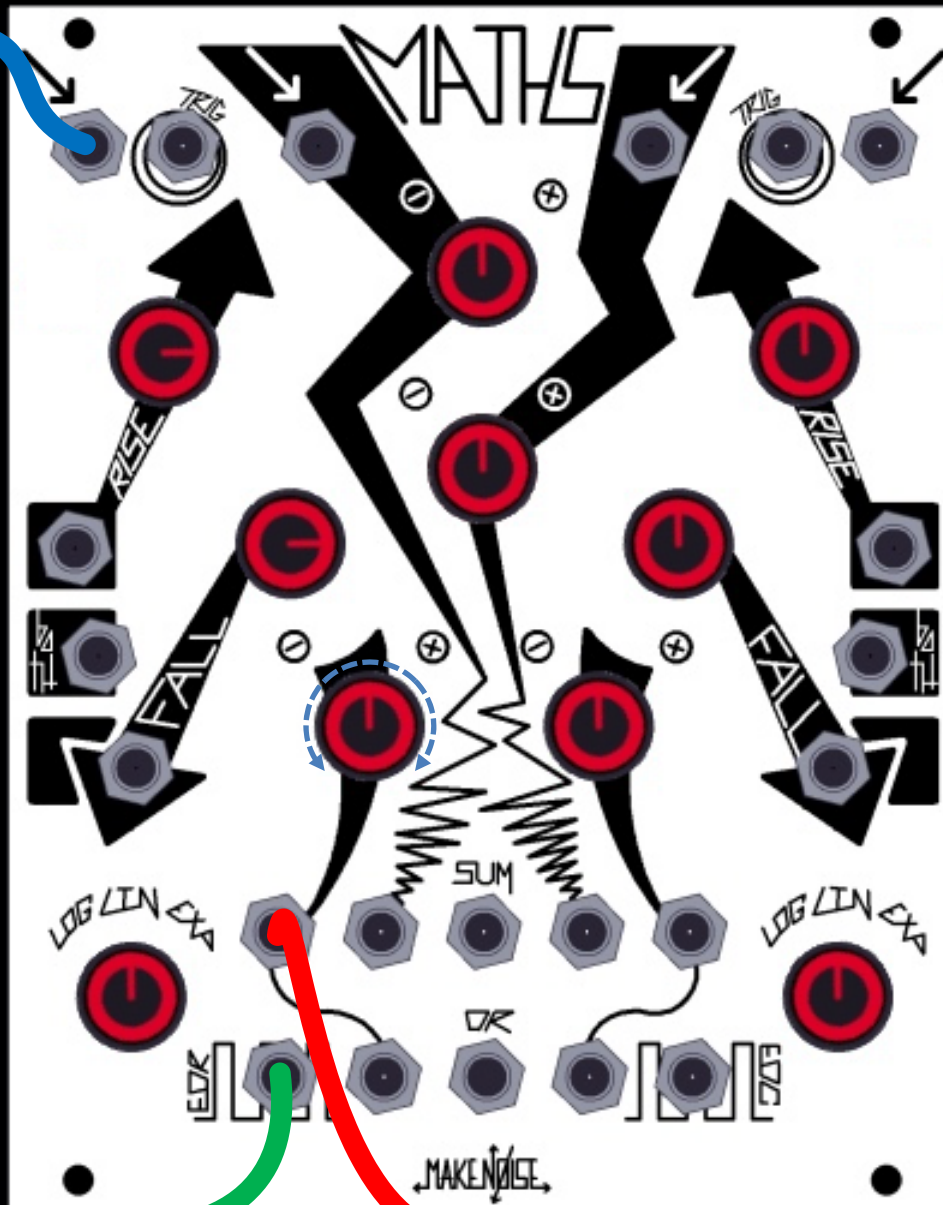
signal(s) to be added



Out

Peak Detector

signal to be detected

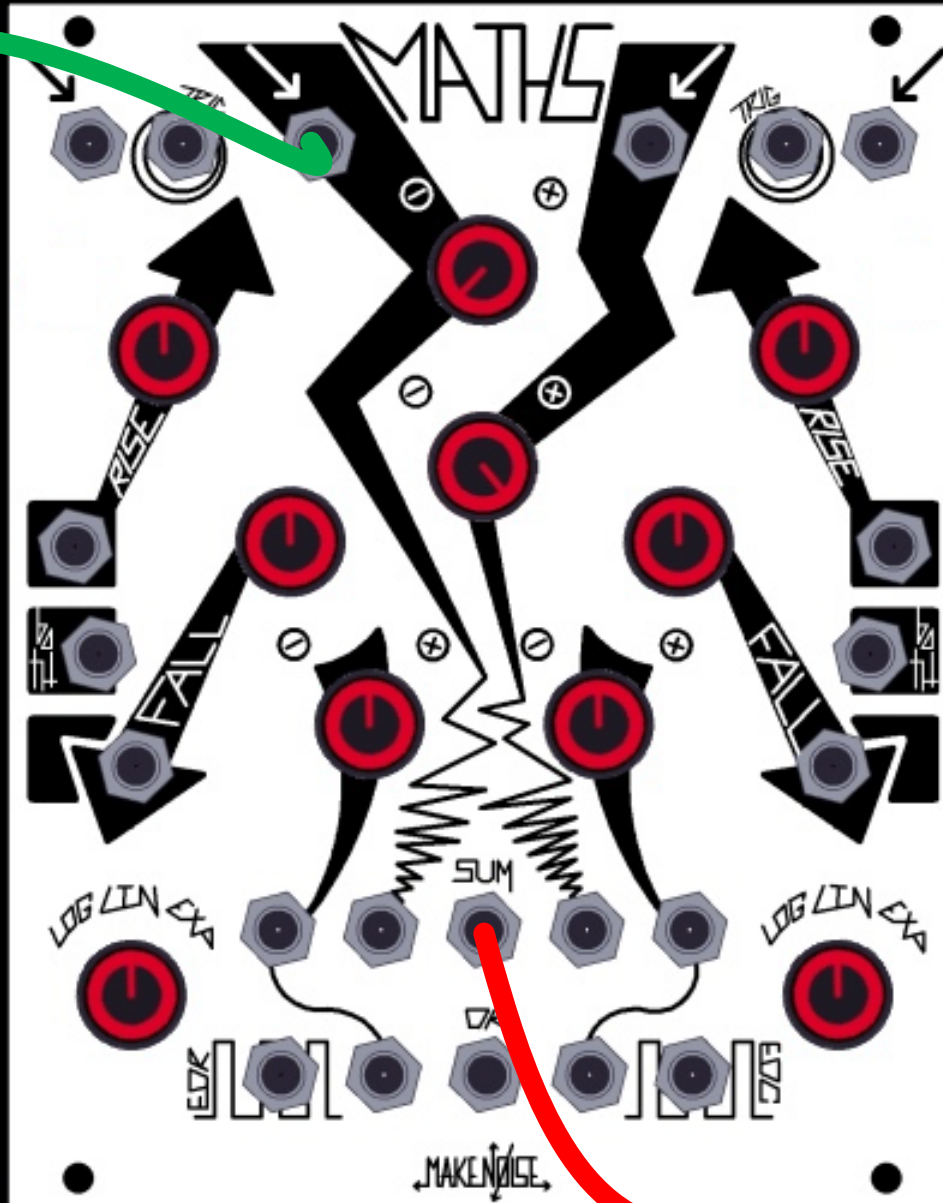


Gate Out

Out

Voltage Mirror

control signal
to be mirrored



Out

Multiplication

positive control
signal to be
multiplied

positive multiplier
control signal

Out

Out

